# An improved ZVS half-bridge DC-DC converter using an auxiliary switch

ISSN –1817 –2695

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**((Received 7/6/2009, Accepted 13/12/2009))**

## *ABSTRACT*

Presented in this paper is a high frequency DC-DC converter with output isolation and soft switching (Zero Voltage Switching (ZVS)) using an auxiliary switch and output resonant network: ZVS with proper core reset was achieved through the resonance that exists between the magnetizing inductance and the parasitic capacitance. All switches are operated at ZVS with minimum current and voltage stresses. The steady state analysis and basic design considerations are given to explain the principle of operation, using Matlab software (v.7)
**Keywords:** DC-DC Converters, Zero Voltage Switching, Zero Current Switching, auxiliary Switch

## *1. Introduction*

DC-DC Converters are widely used in different type of electronic equipments such as industrial and medical X-ray imaging [1]. However, the design of DC-DC converter is problematic because the large turns ratio of the transformer exacerbates the transformer non-idealities, as well as that the transformer has to be reset during the transistor off-period, which usually results in higher voltage stress across the switch due to the energy stored in the magnetizing inductor and higher turned-off losses due to the overlap between the voltage and the current of the switch. Thus, when the switch is turned on, the energy stored in its output capacitance and the winding capacitance of the transformer is dissipated in the semiconductor devices, which result in high turn-on losses [2]. On the other hand, an additional reset circuit with voltage clamp should be employed and sufficient time interval of reset time should also be provided in the practical converter [3]. Several schemes have been proposed to solve this problem, including such techniques as resistor- capacitor- diode (R-C-D) clamp, active clamp, extra winding reset etc... [4]. Soft switching is another possibility to reduce the losses in power electronic switches. Actually, the operation of power electronic switches in ZVS-mode (zero-voltage-switch) or ZCS-mode (zero-current-switch) is called “soft switching”, conventional resonant converters such as parallel resonant converter (PRC), series resonant converter (SRC) and inductor-capacitor-capacitor (LCC) type Quasi-resonant-converter(QRC) were several schemes which are used to achieve soft switching topology [5].

ZVS and ZCS techniques have been proposed to reduce the switching losses without increasing the current and voltage stresses [5].

In this work, DC-DC converter with soft switching, output isolation, analysis and design will be achieved. ZVS can be achieved by using a small network in parallel with the secondary winding and allowing anti-parallel diode of the switch to conduct before turning-on. Resonance occurs between the magnetizing inductance and the resonance capacitance including both the output capacitance of the transistor, transformer winding capacitance and the junction capacitance of the diode. An additional winding and diode clamp network is used to clamp the voltage stress to the reflected output voltage in the primary side of the transformer. The converter transfers the magnetizing energy to the load during the transistor off-period. It will be shown that all switches operate at soft-switching in the wide range and the voltage and the current stresses will be kept at the minimum values.

## *2. The Operation of the Classical Soft switching DC-DC converter*

Figure (1) shows the circuit diagram of the classical soft switching DC-DC converter[6]. The circuit consists of two switches, the first switch ($S_1$)is connected in parallel with both capacitor ($C_1$) and diode ($D_1$); the second switch ($S_2$) is connected in parallel with both capacitor ($C_2$) and diode ($D_2$), then connected in series with the primary winding of the transformer to allow the core to reset.$C_2$ is the resonant capacitor incorporated with the parasitic output capacitance of switch ($S_2$). The transformer provides electrical isolation and energy transfer from the inductor ($L_i$) to the output circuit which is composed of rectifier diode ($D_s$), filter capacitor ($C_o$) and load resistor ($R_o$). ($L_m$) is the magnetizing inductance of the transformer[7].

In steady state analysis of conventional DC-DC converters, there are three equivalents topological stages and key waveforms for one switching period shown in figure (2) and figure (3), respectively.

Stage (1) [$t_o$-$t_1$]: $S_1$ is turned-off and $S_2$ is turned-on. The voltage across $S_1$ is the reflected output voltage $nV_o$ and the current ($i_{ds2}$) through $S_2$ linearly decreases. The energy stored in $L_m$ will be delivered to the load over the transformer(T), forcing $D_s$ to conduct while magnetizing energy increases due to the linearly increase of $i_{Lm}$ During this period. $i_{lm}$ and $i_{ds2}$ are given by [7]:

$$i_{Lm}(t) = \frac{nV_o}{L_m}[t - \frac{1}{2}(1-D)T_s - t_o] \quad (1)$$

$$i_{ds2}(t) = \frac{V_{in} - nV_o}{L_i}(t - t_o) + I_{Li}(t) \quad (2)$$

Where D is duty ratio of $S_1$, $T_s$ is the switching period.

Stage (2) [$t_1$-$t_3$]: At $t_1$, $S_1$ turned on while $S_2$ is turn-off. $i_{Li}$ linearly increases and $L_m$ and $C_2$ forms together resonant tank. Hence,$V_{ds2}$ and $i_{Lm}$ at resonant are sinusoidal waveform. During the period ($t_1$-$t_2$), the magnetizing energy is transferred to $C_2$ while at the period ($t_2$-$t_3$) this energy transferred from $C_2$ into $L_m$ as shown in figure (3). In this period the voltage stress across $S_2$ reaches its maximum value, $i_{Lm}$ and $v_{ds2}$ can be expressed as[7]:

$$i_{Lm}(t) = \frac{nV_o(1-D)T_s}{2L_m}\cos\omega_o(t - t_1) \quad (3)$$

$$i_{ds2}(t) = \frac{nV_o(1-D)T_s}{\sqrt{L_m}C_2}\sin\omega_o(t - t_1) \quad (4)$$

where $\omega_o = \frac{1}{\sqrt{L_m C_2}}$

Stage (3) [$t_3$-$t_4$]: $D_3$ is turned-on at $t_3$ and it is at ZVS. $i_{lm}$ flows through $D_2$ to keep ZVS across $S_2$ , so that $S_2$ can be turned-on at $t_4$. Finally, at the $t_4$ time $S_2$ is turned-on and $S_1$ is turned-off, again to start a new cycle.

From the above steady-state analysis, it can be shown that the voltage and current stresses of $S_1$ is given by [7]:

$$v_{ds1\max} = nV_o \quad (5)$$

$$I_{d1\max} = \frac{I_o}{n} + \frac{nV_o(1-D)T_s}{2(L_i)} \quad (6)$$

However, figure (3), shown that the maximum voltage stress across $S_2$ can be given by:

$$V_{ds2\max} = n\pi V_o(1-D)\frac{\omega_o}{\omega_s} \quad (7)$$

Where $\omega_s = 2\pi f$ is the switching frequency

Equation (7) can be rewritten as follows:

$$v_{nc} = \frac{v_{ds2}}{nV_o} = \pi(1`-D)\frac{\omega_o}{\omega_s} \quad (8)$$

Where $v_{nc}$ is the normalized voltage stress.

Therefore, the condition for ZVS operation of $S_2$ can be expressed as:

($\omega_{ns} < 2D$) (9)

Where $\omega_{ns} = \omega_s / \omega_o$ is the normalized frequency

Figure (4) shows the relationship between the normalized voltage stress ($v_{nc}$) and the normalized frequency ($\omega_{ns}$). ZVS region can be verified at the region when ($\omega_{ns} \prec 2D$) and then the minimum voltage stress across $S_2$ can be obtained. The diode $D_s$ is in reverse block state when $S_2$ is in the off-state. The maximum voltage stress across $D_s$ occurs at $t_2$, is given by[7]:

$$V_{Ds\max} = V_o[1 + \pi(1-D)\frac{\omega_o}{\omega_s}] \quad (10)$$

From the above analysis, it can be seen that $S_1$ operates at hard switching, while $S_2$ can operate at ZVS region. Furthermore, the voltage stress across $S_2$ will be relatively high and it is difficult to optimally design this converter to maintain ZVS operation and keep minimum voltage stress of $S_2$.

In the following section. An improved converter will be presented to show that the converter will operate at ZVS in full load range while the voltage and current stresses will be kept at the minimum [7].

## *3. The operation of the improved isolated DC-DC Converter*

To simplify the analysis, assume that the filter capacitor ($C_o$) is sufficiently large so that the output voltage ($V_o$) can be considered as a constant. Figure (5,6 and 7), show the circuit diagram, the key waveforms and the eight stage of the improved ZVS isolated converter, respectively.

An extra winding ($N_r$) and diode ($D_r$) network are employed to reset the core, suppress the voltage stress across $S_2$ and transfer partial magnetizing energy to the load. A small network consisting of an auxiliary switch ($S_a$), diode ($D_a$), resonant inductor ($L_r$) and resonant capacitor ($C_r$) are employed to achieve ZVS of $S_1$. In steady-state operation, eight topological stages exist as shown in figure (8) within one switching period.

- Mode (1) [$t_o$-$t_1$]: $S_1$ is turned-on and $S_2$ is turned-off at $t_o$. Diode ($D_r$) is off while Diode ($D_s$) is conducting. The energy is delivered to the load through the isolated transformer during this time interval. $S_1$ current is given by

$$i_{ds2}(t)=\frac{V_s-nV_o}{L_i}(t-t_o)+I_{Li}(t_o) \quad (11)$$

- Mode (2) [$t_1$-$t_2$]: At $t_1$; Auxiliary switch $S_a$ is turned-on. The current through the inductor ($L_r$) linearly ramps up to reaching $I_o$ while the current through $D_s$ will be naturally turned-off at $t_2$ when $i_L=I_o$, this period is given by

$$t_{12}=\frac{I_o}{V_o/L_r} \quad (12)$$

- Mode (3) [$t_2$-$t_3$]: At $t_2$ $L_r$ and $C_r$ form a resonant tank. The resonant capacitor $C_r$ discharges while the current through $L_r$ continues to increase in sinusoidal form during this period. $C_r$ can be considered as the combination of the output capacitance of $S_1$ and the transformer winding capacitance reflected in the secondary side. The resonant voltage and current can be expressed as:

$$v_{cr}=V_o\cos\omega_{o2}(t-t_2) \quad (13)$$

$$i_{Lr}=I_o+\frac{V_o}{Z_o}\sin\omega_{o2}(t-t_2) \quad (14)$$

where $\omega_{o2}=\frac{1}{\sqrt{L_rC_r}}$ , $Z_o=\sqrt{\frac{L_r}{C_r}}$

At $t_3$ the energy stored in these parasitic capacitors is completely transferred to $L_r$, where the voltage $v_{cr}$ and $v_{ds2}$ decreases to zero and $D_1$ begins to conduct. This time interval is determined by: $t_{23}=\frac{\pi}{2}\sqrt{L_rC_r}$ Where $C_r=C_1+C_{tr}+C_j$. $C_{tr}$ and $C_j$ are the parasitic capacitance of the transformer and the junction capacitance of $D_s$.

- Mode (4) [$t_3$-$t_4$]: $D_1$ is turned-on and $S_1$ conducts at $t_3$. ZVS in this period is achieved. $L_r$ current flows through the secondary winding as a constant.

- Mode (5) [$t_4$-$t_5$]: At $t = t_4$, with $S_a$ and $S_2$ both on and $S_1$ is turned-on, the current through $L_r$ decreases to zero while the voltage across $S_a$ clamps up to $V_o$ due to the conduction of $D_a$. In this case, the energy stored in $L_r$ will be transferred to the load. On the other hand, the magnetizing inductance ($L_m$) and the capacitance ($C_2$) form a resonant circuit. This period ends when $v_{ds2}$ ramps up to ($nV_o$) where clamped diode ($D_r$) begins to conduct at ZVS.
- Mode (6) [$t_5$-$t_6$]: $D_r$ is turned-on when ($t = t_5$), $v_{ds2}$ is clamped at ($nV_o$) where (n) is turn ratio. The energy stored in ($L_m$) is transferred to the load through the winding $N_r$ and $D_r$. it is shown that the primary winding is applied a negative reflected output voltage which resets the transformer core as shown in figure (6). When this period is completed, $i_{Lm}$ is equal to zero, and it linearly decreases at a rate( $-nV_o/L_m$). $i_{Lm}$ is given by:

$$i_{Lm}(t) = \frac{-nV_o}{L_m}(t - t_5) + I_{Lm}(t_5) \quad (15)$$

- Mode (7) [$t_6$-$t_7$]: At the beginning of this period, $i_{Lm}$ decreases to zero and $D_r$ is turned-off at zero-current. $C_2$ and $L_m$ form a resonant tank. The energy stored in $C_2$ is transferred to $L_m$, which makes the $i_{Lm}$ becomes negative at $t_7$. When $t = t_7$, $D_2$ is turned-on and $v_{ds2}$ decreases to zero. In this period the current $i_{Lm}$ and the voltage $v_{ds2}$ are given by:

$$i_{Lm}(t) = \frac{-nV_o}{\sqrt{L_m/C_2}} \sin \frac{1}{\sqrt{L_m C_2}}(t - t_6) \quad (16)$$

$$v_{ds2}(t) = nV_o \cos \frac{1}{\sqrt{L_m C_2}}(t - t_6) \quad (17)$$

- Mode (8) [$t_7$-$t_8$]: At $t_7$, $v_{ds2}$=0. The current $i_{Lm}$ remains constant by flowing through the anti-parallel $D_2$. As a result, $S_2$ can operate at ZVS when it is turned on at $t_8$.

## *4. Design Considerations and Simulation Results of the proposed scheme*

Several design considerations should be taken into account. First, duty ratio of $S_1$ is restricted to greater than 0.5 so that the transformer has sufficient time interval to be reset. Second, the resonant period between $L_m$ and $C_2$ should be chosen less than one-tenth of the switching period to achieve ZVS of $S_2$. The delay time between the turn-on signal of $S_1$ and $S_a$, $t_d$, has to meet the following:

$$t_d \geq \frac{I_o}{V_o/L_r} + \frac{\pi}{2}\sqrt{L_r C_r} \quad (18)$$

So that $S_1$ can be turned on at ZVS.

the following values are been considered in the design procedure:

a) switching frequency is 200kHz

b) $N_p$=15 , $N_r$=12 , $N_s$=12

c) $V_{in}$= 200 volt

d) $R_o$= 270 Ω

e) From figure (4) by using $\omega_{ns}$ =2D, the Circuit parameters are : $L_i$= 1 mH, $L_m$=1, mH , $L_r$= 8 µH ,$C_1$=$C_2$= $C_3$=400µF

Figure (8) show the matlab circuit simulation. Figure (9) shows the waveforms obtained using this Simulation and figure (10) shows an efficiency of about 82% -88%. These figures show that all Switches Operate at ZVS and the Waveforms are in a good agreement with steady-state analysis.

## *5- Conclusions*

An improved Zero Voltage Switching modified boost converter with output Isolation using a small network in parallel with the secondary winding of the transformer is presented. The result obtained from this modified circuit maintain that this model has better efficiency compared with the previous model due the elimination of the stresses on the switches using the auxiliary switch.

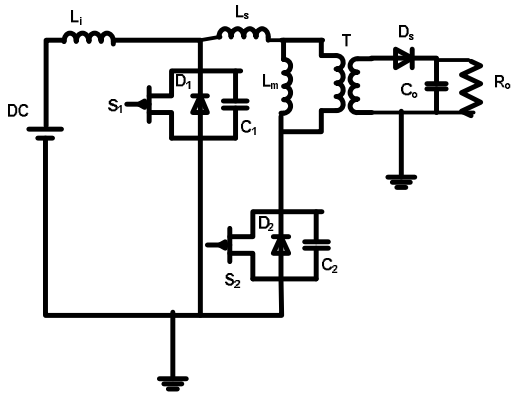


Figure (1): The classical DC-DC Converter Circuit

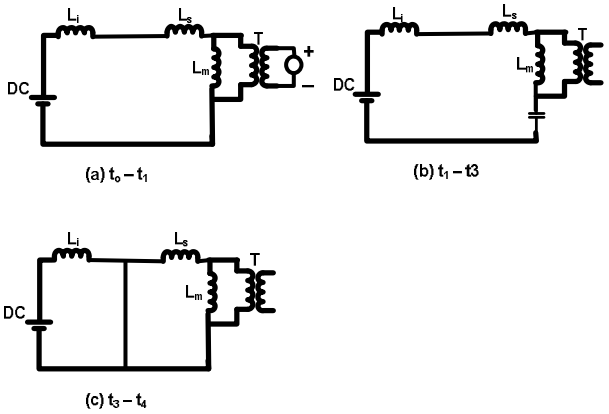


Figure (2): Three Equivalent topological Stages of the classical DC-DC converter circuit

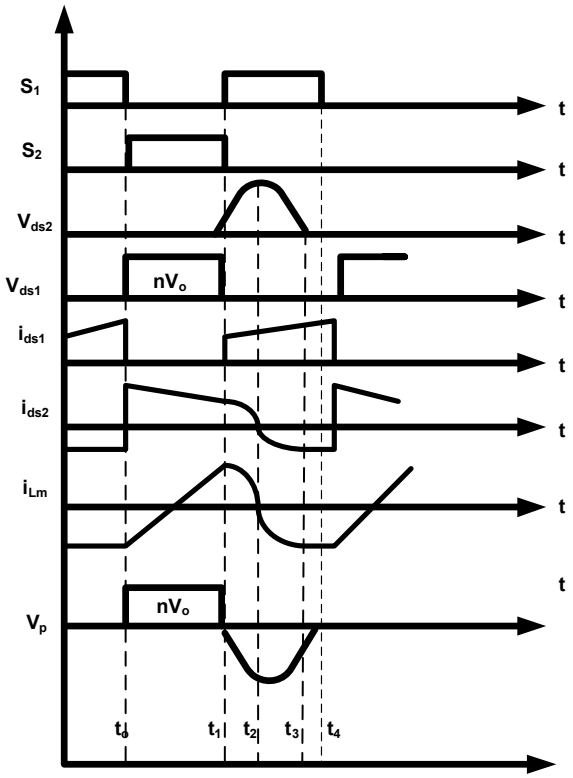


Figure (3): key Waveforms for Fundamental DC-DC Converter, exist over one switching period

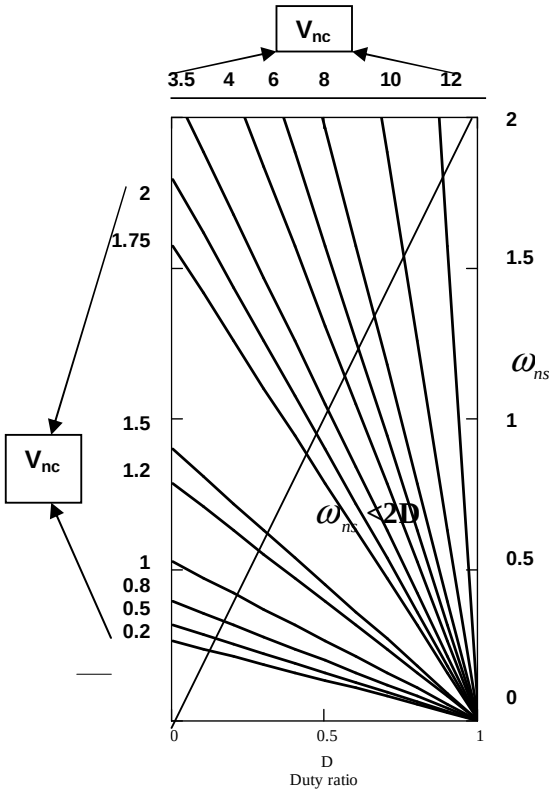


**Figure (4) :The relationship between $\omega_{ns}$ and ( D)**

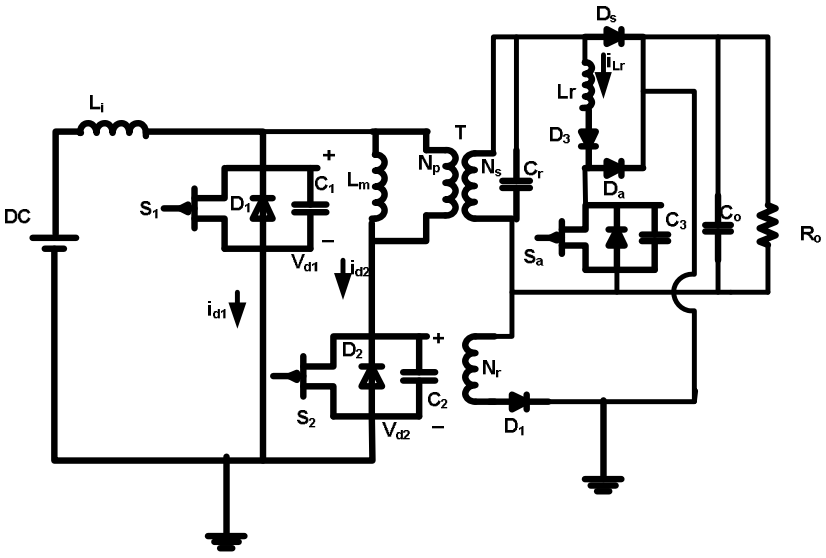


**Figure (5): Circuit Diagram of the Improved DC-DC Converter.**

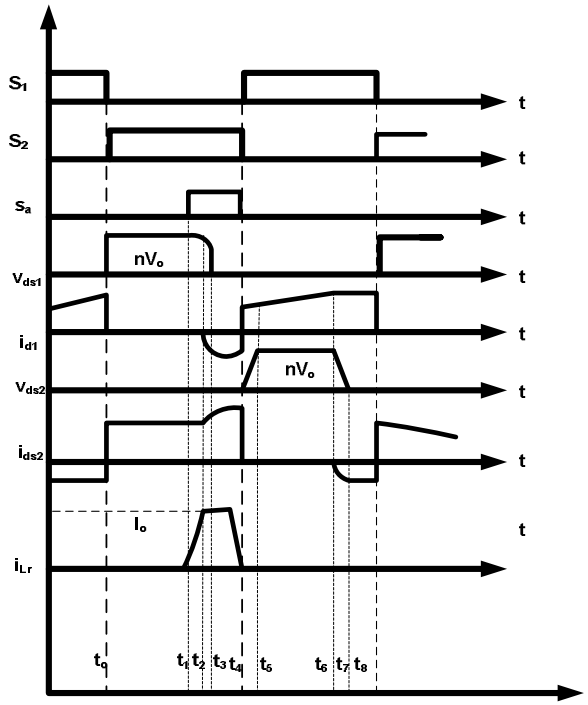


**Figure (6): Key waveforms of the improved ZVS isolated converter**

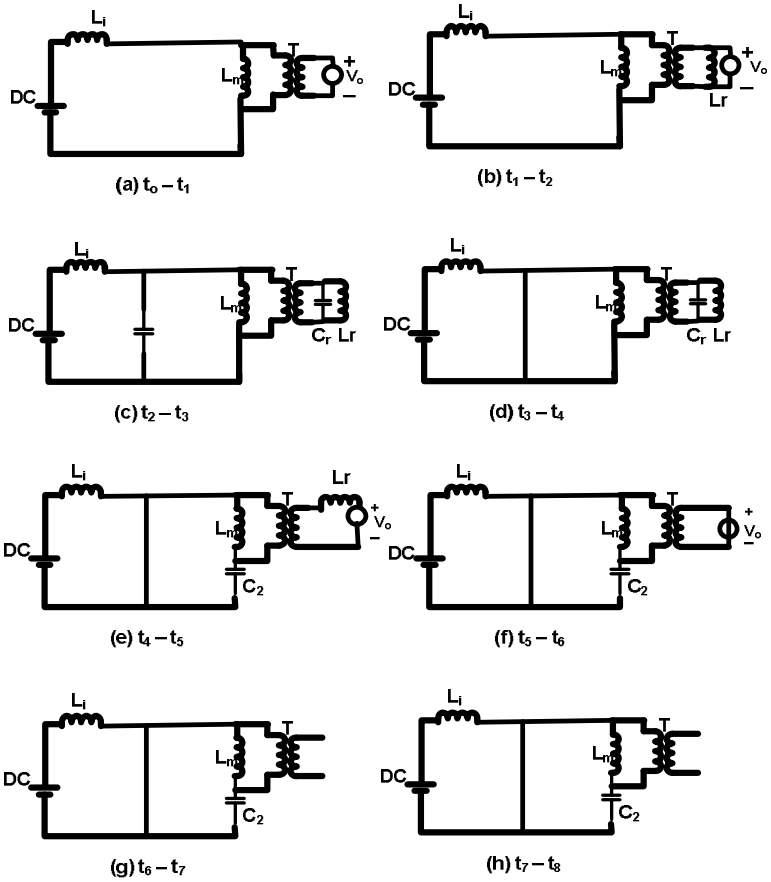


**Figure (7): Eight stages of the improved**

**DC-DC Converter within one switching period.**

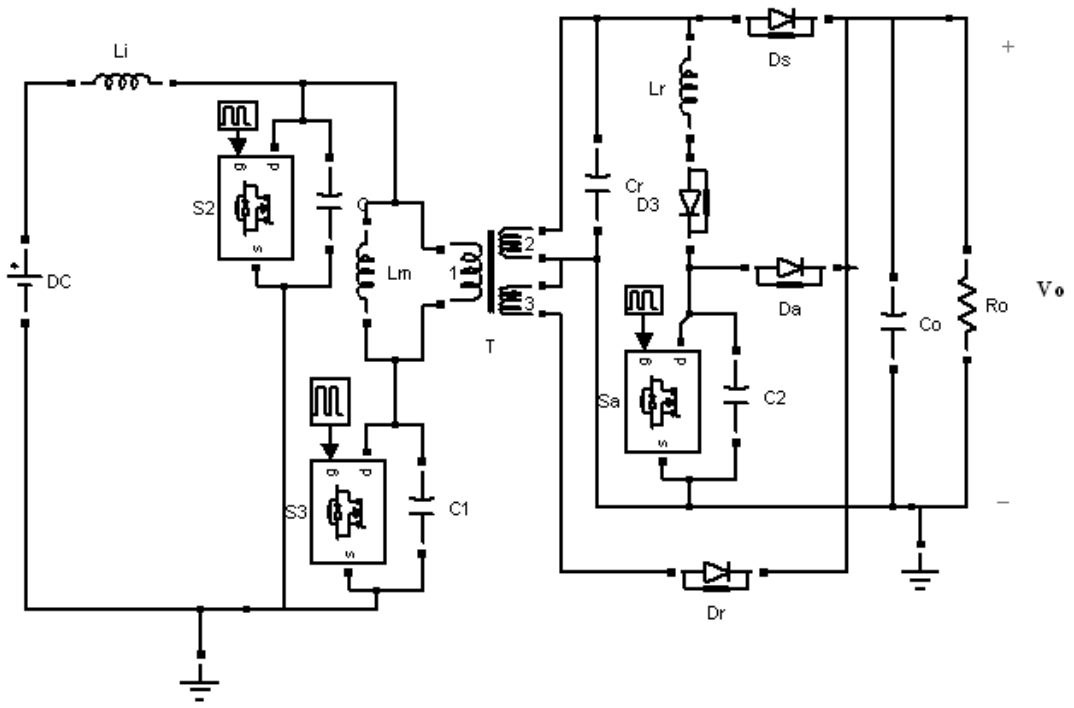


**Figure (8): The implementation of improved DC-DC Converter Circuit using Matlab Program**

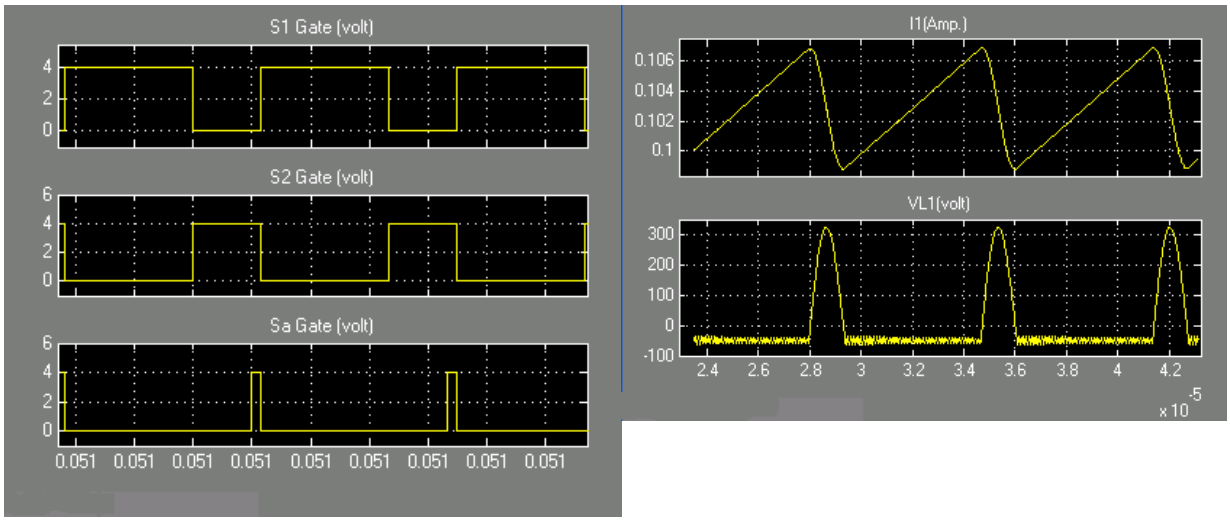


**Figure (9): Simulation Key Waveforms of the improved DC-DC Converter.**

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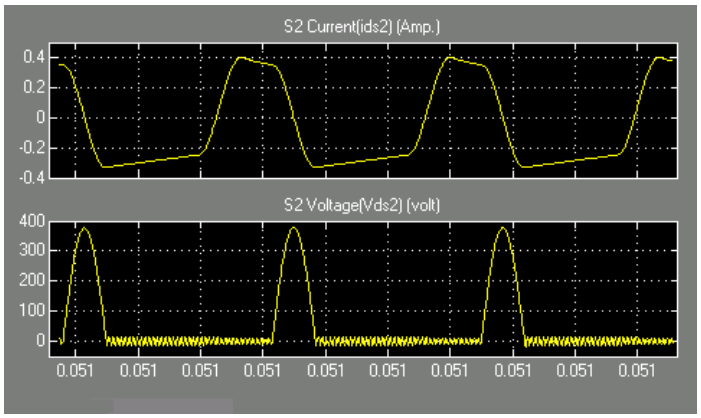


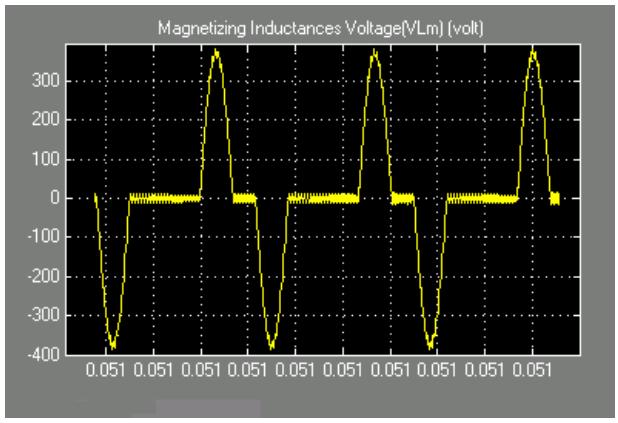


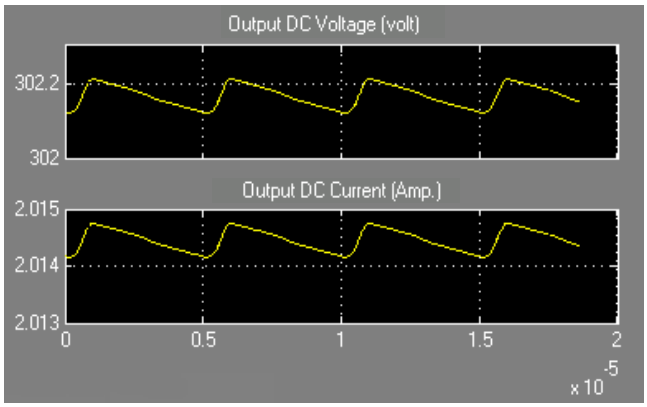


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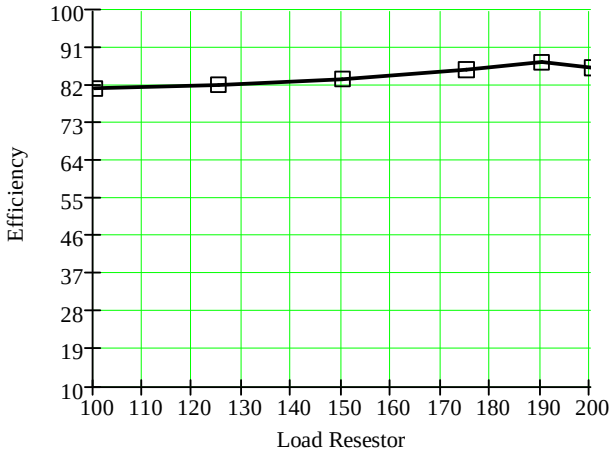


**Figure (10): The efficiency versus the load resistor**

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## محول قدره مستمر–مستمر نصف قطري ذوالتوصيل الصفري محسن بأستخدام مفتاح مساعد


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***مركز الحاسبة الالكترونية***

***جامعة البصره***



***المستخلص:***

يستعرض هذا البحث أنموذجا محسنا" لمحول الفولتية (DC-DC) بأستخدام الترددات العالية مع دائرة خرج معزولة وبأستخدام تقنية المفاتيح الناعمة (التوصيل الصفري للفولتية)و أستخدام مفتاح مساعد ودائرة رنين خارجية لانجازالتوصيل الصفري للفولتية . اتمام عملية التوصيل الصفري للفولتية واعادة وضع الملف الابتدائي للمحولة يحصلان عند حالة الرنين وهذه الحالة تقع بين المحاثة المغناطيسية ومتسعة المفتاح. ان الفولتية والتيار على المفتاح سيكون اقل ما يمكن.

التحليل الرياضي و الاعتبارات الاساسية للتصميم ساهمت في توضيح مبدأ العمل لهذه الدائرة. بالاستعانة ببرنامج ال(Matlab)حيث وجد تطابق جيد بين النتائج النظريه وبين النتائج التي حصل عليها من البرنامج المذكور .