The Electrical Characteristics of Inverted Coplanar Field Effect Transistor Doping With Indium Fabricated by Spray Pyrolsis Technique (SPT)

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ISSN –1817 –2695
(Received 22/9/2002, Accepted 26/1/2004)

Abstract

Inverted coplanar type field effect transistor has been fabricated using (SPT) .The electrical characteristic of the device which is investigated at room temperature and in the dark, show the characteristics increased in the source – drain current due to doping the CDS layer with indium. The electrical characteristics were investigated through measuring output and transfer characteristics.
The result shows that device with low threshold voltage was corresponding to indium doped with concentration 0.05.The incremental of source-drain current due to IN general Indium dopant was found to to improve the electrical characteristics of the device compare with undoped one.

Key Words: Electrical, Inverted Coplanar FETs,Spray Pyrolsis Technique (SPT) .

Introduction

The use of inorganic materials in electronic device has still considered a commercial although discovery new materials such as polymers which were previously depend elsewhere [1].
In such device ,the effective layer was separated by insulating layer from gate electrode.
Different techniques have been used in fabrication and studying the electrical characteristics of thin film effect transistor [2].One at the most easy and low coast technique steps in their fabrication [3].It is well known that thin film field effect transistor is essentially the same as the metal oxide semiconductor FET but it's differs only in the materials and construction method[4].The researches in this field takes tow main branches ,first :is to seek a new material to having a proper electrical characteristics which serve either as insulating or effective layer ,second :is to fabricate the device using easy and efficient technique .Accordingly the results obtained from studying the electrical characteristics of the devices is based on satisfying the later condition.In this study inverted coplanar FETs has been fabricated using CdS in as effective layer .The whole device was fabricated using (SPT) technique .The electrical characteristics were investigated by measuring both output and transfer characteristics of the devices in the room temperature.

Experimental Procedure

In CdS/Fe_2O_3 FETs of the inverted coplanar configuration has been fabricated applying the following procedure:

Metal layer as a gate electrode was evaporated on the glass substrate by evaporation aluminum under low pressure 10^{-4} toor .Fe_2O_3 thin film acts as insulating layer was deposited on the gate electrode using spraying pyrolysis technique(SPT) .The details of spraying conditions were similar to that previously depend elsewhere [5].Source and drain aluminum electrodes with fingure shape has been deposited on the insulating layer using evaporation technique .The electrodes has the dimension (length 2.5mm , width 5mm) and separated by 5mm .The fabrication process was terminated by deposition the semiconducting thin layer of cadmium sulfide as an active layer using again (SPT) with similar spraying condition which has been depend elsewhere [6] as shown in figure(1).Other devices have been fabricated using semiconductor layer doped with indium with different concentration 0.01,0.03 and 0.05.The electrical characteristics of the devices have been investigated at room temperature and in a dark using shielded box .

Results and Discussion

The thickness of source ,drain and gate electrodes were (3mm) ,the Fe_2O_3 and CdS thin films were measured with digital micrometer model Mintest FD 1250 and found to be (1μm).Thin films with (1μm) thickness did exhibit smooth black surfaces and were free from holes . The coating surface roughness of thin films with increasing their thickness above (1μm) ,thus may be due to the presence of any significant barrier at the metal /semiconductor interfaces (at the region under source –drain connection) which would give a current (I_{ds}) limited by the film resistance .Figure (2) shows the output characteristics of the device measured at R.T with gate-source voltage (Vgs=10 V) .It was observed that increasing concentration has lead to a pronounce effect on increasing source-drain current ,then it tends to saturate for concentration in the range (0.05-0.1) and these were attributed to the full all the cadmium holes .Figure(3) was include the behavior of free doped layer for a comparison .the indium dopant was noticed to increase the current about four order of magnitude in the saturation region(In=0.05).Pinch –off voltage that the drain current reaches the saturation has been recorded and found to be increasing the dopant concentration as shown in Figure(5) .Generally all the curves show a similar characteristics .In the high dopant concentration ,three region can be identified clearly (1) the liner region ,(2) exponential region , (3) saturation region .Ohmic behavior was identified in the low voltage region ,where a deviation from ohm law was terminated in the pinch –off voltage ,where a saturation characteristics has been started .The transfer characteristics of the devices which shown in Figure(2) has also show a pronounce effect due to indium dopant effect .

In order to calculate the threshold voltage ,the relationship of square root of drain current vs. gate voltage has been drawn as shown in Figure (4).Threshold voltage V_T has been calculated by connecting drain and gate electrode using similar method employed elsewhere [7] with help of the following relationship:

$$I_{ds}^{1/2} = [(W/2L)\, C_i\, u_{FE}]^{1/2} (V_{gs}-V_T) \quad \ldots(1)$$

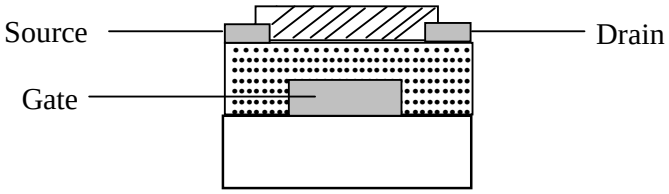
Where :W,L,C_i , u_{FT} and V_{gs} are channel width ,channel length, capacitance per unit area ,charge carriers mobility and gate voltage respectively.

The relationship(1) shows the plot of square root of drain current as a function of the gate voltage (V_{gs}) ,which is gives a straight line then the intercept of a straight line occurs at a threshold voltage(V_T) ,the slop of this straight line was used to calculate the charge carriers mobility u_{FT} and found equal to (u_{FT} =1.1 $cm^2.V^{-1}.sec^{-1}$) .Figure (4) and Table (1) shows that higher indium dopant has a higher threshold voltage (V_T =0.5 V).On other hand the electrical characteristics of these devices have a similar characteristics to the Metal-Oxide FET devices [8] .the incremental of source – drain current due to increasing the indium concentration can be explained by increasing the channel conductance of the device due to the effect of dopant which act as a donor dopant as has been previously discussed elsewhere[9].

Table(1):Show the threshold voltage for In:CdS/Fe_2O_3 inverted coplanar type

Indium co ncentration%	Threshold voltage(V)
0	1
0.01	0.7
0.03	0.55
0.05	0.5

Caption of Figures



Semiconductor(CdS)

Dielectric (Fe_2O_3)

Aluminum electrode

Figure (1): In:CdS/Fe_2O_3 FET inverted coplanar type preparation by (SPT)

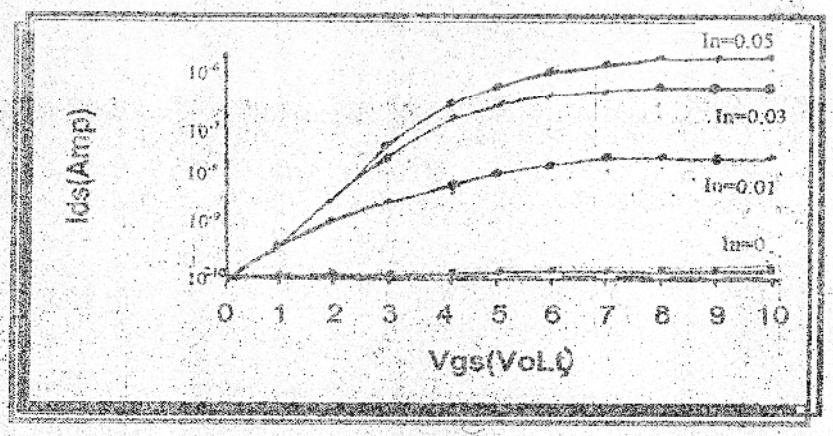


Figure (2): Show the transfer characteristics of In:CdS/Fe_2O_3 FET_s Inverted coplanar type at Vds=5volt

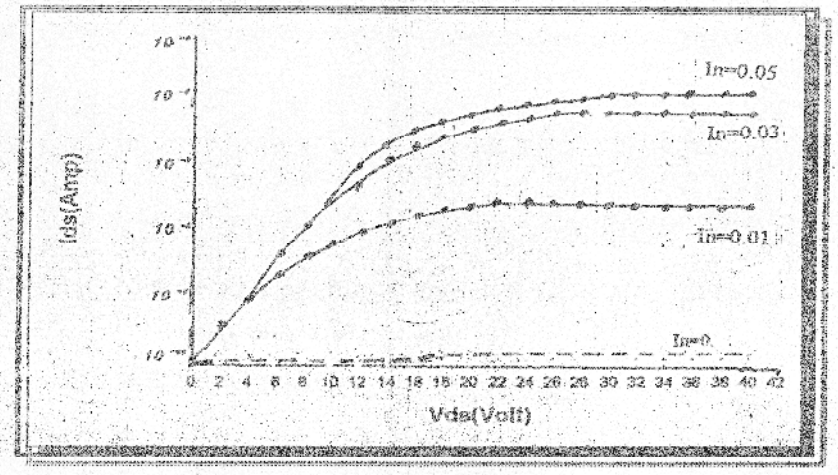


Figure (3): Show the OUTPUT characteristics of In:CdS/Fe_2O_3 FET_s inverted coplanar type at Vgs=10 Volt

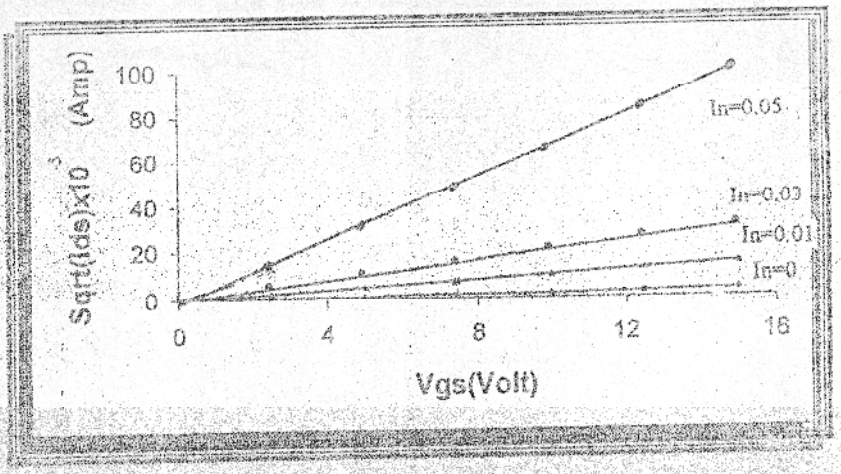
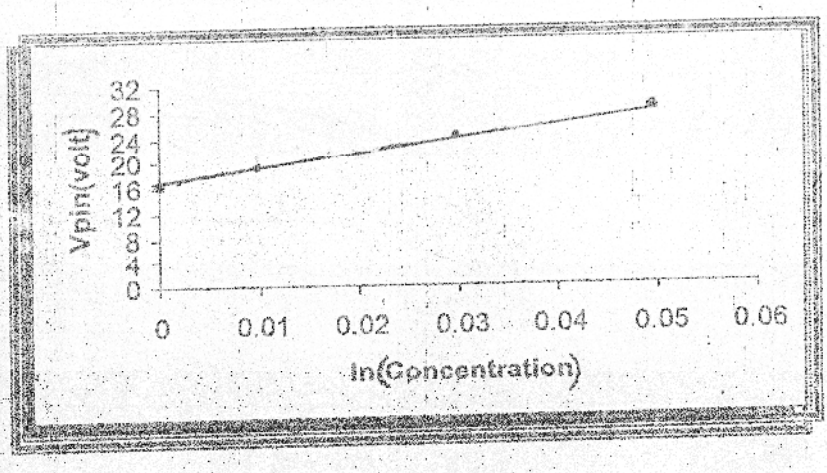


Figure (4): The relationship between the squre root of drain current VS. gate voltage when the gate and drain electrodes connected



Figure(5): Show the relationship between the pinch-off voltage and indium concentration

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الخلاصة

الهدف من هذا البحث هو تصنيع ودراسة الخصائص الكهربائية لترانزستور تأثير المجال نوع Inverter Coplanar المشوب بالانديوم بطريقة الرش الكيميائي الحراري . تم قياس الخصائص الانتقالية والإخراج لهذا النوع من ترانزستور تأثير المجال في درجة حرارة الغرفة وفي الظلام .ومن دراسة هذه الخصائص تبين إن تيار المنبع – المصرف يزداد بزيادة النسبة الوزنية للانديوم المشوب لغشاء شبه الموصل CdS ومن قياس جهد العتبة تبين أن التشويب بالانديوم بالنسبة الوزنية 0.05 يعطي أوطأ جهد عتبة للترانزستور. نتج عن هذا البحث أن التشويب بالانديوم يحسن في أداء الخصائص الكهربائية لهذا النوع من ترانزستور تأثير المجال مقارنة بأخر غير مشوب .