Design and Implementation of Optimal Multi-rate Digital Down Converter Using MALAB and ModelSim

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ABSTRACT

In this paper, a design and implementation of a digital down converter (DDC) filter for GSM, CDMA, WCDMA is presented. A powerful system design tool, Xilinx System Generator is adopted to simplify the design cycle and increase the productivity. The proposed DDC is composed of three stages of cascaded filters. The maximum operation speed of the Proposed DDC filter is 100MHz. The remaining sub-modules of the DDC, such as the FIR filter, is co-designed using MATLAB FDATool and ModelSim with a tradeoff between the receiving path of requirements, algorithm and hardware implementation complexity. The system has been successfully verified using the MATLAB module and ModelSim. The most important stage in the design is the HDL code generation for implementation phase and results verification.

Keywords: DDC, FIR, MATLAB, ModelSim.

تصميم مرشح رقمي خافض متعدد السرعات باستخدام برامج محاكات وتنفيذ حديثة

الخلاصة

يعرض هذا البحث تصميم وتنفيذ مغير رقمي خافض للتردد يدعم منظومات اتصالات مختلفة . لتسهيل واختصار دورة التصميم تم اعتماد ادوات تصميم حديثة مثل مولد النظام . المرشح المقترح يتكون من ثلاثة مراحل لمرشحات رقمية مربوطة مع بعضها بشكل متوالي . السرعة القصوى لهذا المرشح هي 100 ميكا هيرتز . اجزاء المرشح المقترح مثل مرشح الاستجابة المحدودة تم تصميمها باستخدام برنامج محاكات (ماتلاب) و التحقق منها بواسطة برنامج تنفيذ حديث (موديلسم) لتقليل التعقيد في النظام. المرشح المقترح تم التحقق منه بنجاح باستخدام برامج متطورة و معتمدة عالميا. المرحلة الاكثر اهمية في هذا التصميم هي توليد شفرة اللغة الخاصة بجهاز التنفيذ .

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INTRODUCTION

A key part of wireless communication system is the Digital Down Converter (DDC). It can be performed by a dedicated hardware in a processor. For example, when a GSM module is activated and connected to the internet via WLAN, It can be reconfigured in a chip which is used as a DDC to execute multi-tasks. In this case the hardware has a high utilization factor. The algorithm cans be performed continuously and only parameter settings might be changed. Any adaptability and spare performance will not be used in this situation. Currently radio frequency transceivers demand a high integration devices as well as low cost and low power consumptions. The system is able to adapt into multiple communication standards such as software defined radio (SDR)[1]. Several designs that implement decimation filters in SDR have been reported to show the prime importance of the Software. Decimation filter in Global System for Mobile (GSM), Wideband Code Division Multiple Access (WCDMA), 802.11a, 802.11b, 802.11g and Worldwide Interoperability for Microwave Access (WiMAX) are reported in [2]. A multistage sample rate converter of SDR receiver using Equiripple FIR according to Hermann formula was proposed by [3]. Another low passband error in DDC filter with adjacent and rejection of -105dB and -0.05dB passband ripple was reported by [4]. Decimation filter for multi-standard wireless transceivers using MATLAB with -0.1dB in passband ripple and -65dB stopband attenuation for GSM, WCDMA and WLAN was introduced by [5]. Later, a design of multi-standards DDC filter with minimum passband ripple of -0.03dB was produced by [6]. An optimized System Generator based on hardware co-simulation technique to implement GSM in digital down convertor for software defined radios is presented by [7]. The purpose of this paper is to come out with a new technique based on the McClellan-Parks [8] algorithm in designing linear-phase FIR filters with equiripple stopbands as well as an extreme low ripple in the passband and improve the adjacent band rejection requirements.

MATHEMATICAL BACKGROUND

To design the FIR filter, one could start by presenting a table 1 which consist the four types of FIR filters given by [1]. The filter length M is selected to be filter order N divided by 2 assuming Filter type I is used. Then, the frequency response F(θ) of FIR filter is 1 in this case.

In order to minimize the error, an error function $E(\theta)$ related to a weight function $W(\theta)$ is defined as:

$$E(\theta) = W(\theta)[A_d(\theta) - A(\theta)] \quad \ldots \quad (1)$$

where $A_d(\theta)$ is the desired amplitude response, and $A(\theta)$ is the actual amplitude response. A simple weight function $W(\theta)$, could be defined as follows:

$$W(\theta)=\begin{cases}1, \theta \in (passband)\\ 0, \theta \in (stopband)\end{cases} \quad \ldots(2)$$

And the resulting amplitude response, A(θ) is defined by

$$A(\theta)\ \theta \square F(\theta)\ G(\theta) \quad \ldots(3)$$

and

$$G(\theta \square) = \sum_{k=0}^{M} b[k]\cos(k\theta) \quad \ldots(4)$$

where *F(θ)* and *M* are taken from Table 1. The problem is to find the coefficients of *b[k]* that are able to minimize the maximum amplitude of weight error |E(θ)|, where the value can be obtained from the function of:

$$\varepsilon = \square \max|E(\theta)| \quad \ldots(5)$$

where θ □is in the filters' range of operating frequency.

2.1-The Alternation Theorem

The alternation theorem [1] states that there are frequency deviation exist when K □□ 2 frequenciesθ_i, {0 ≤i ≥□ K+ □1}where the maximum error, ε, occurs. That is,

$$|E(\theta_i)| = \varepsilon, \quad 0 \le i \le K+1 \quad \ldots(6)$$

And

$$E(\theta_{i+1}) = -E(\theta_i); \quad 0 \le i \le K \quad \ldots(7)$$

Equation (7) shows that the sign changes for every K+1, resulting in an oscillation or ripple on the band of interest.

2.2-The Remez Exchange Algorithm:

The most famous of the Remez Exchange Algorithm is the version introduced by Parks, and Rabiner [3]. The objective is to find the coefficients b[k] that can minimize □. It uses the properties of the Alternation The
The first step is to find the N order of the desired filter. The following is the empirical formulae that is proposed by Kaiser [9] .

$$N = \frac{-10\log_{10}(\sqrt{\delta p \delta s})-13}{2.32|\theta_p-\theta_s|} \quad \ldots(8)$$

Where:

θ_p is the passband-edge digital frequency,
θ_s is the stopband-edge digital frequency,
δ_p is the passband allowed deviation,
δ_s is the stopband allowed deviation,

and

$$\delta_p = \frac{10^{A_p/20}-1}{10^{A_p/20}+1} \quad \ldots (9)$$

$$\delta_s = 10^{-A_S/20} \quad \ldots (10)$$

where A_p and A_S are the attenuations on the passband and stopband respectively. The stopband and passband energy in this case is given by

$$E(\theta) = \frac{1}{2\pi}\int_F^{\pi} |A_d(\theta)|^2 d\theta \quad \ldots(11)$$

The multistage decimator block diagram is shown in Figure (1). The 5-stage cascaded integrated com (CIC) filter is able to process the high-rate input signal and decimate it by a programmable factor. Then the output from CIC filter will enter into a 21-tap compensator FIR (CFIR) filter that equalizes the "droop" due to the CIC filter and provides further lowpass filtering and decimated by 2. After that a 65-tap programmable FIR (PFIR) filter is used for a final stage decimate-by-2. Note that in a multistage decimator, always put the simplest filter at the early stage in order to make sure that the system is working at the highest rate, then followed by a progressively increase the complexity of the filters in subsequent stages. This is exactly what happens here, the CIC filter is attractive at very high rates because it could work with the multiplier less process. The filter is of a lowpass type using adder and delay units. The magnitude response of the CIC filter is very far from an ideal filter and exhibits a sharp attenuation in the passband which progressively attenuates signals. The CFIR filter is also relatively simple, having only 21 taps which is used to compensate the sharp attenuation from the CIC filter. The PFIR filter is the most complex filter in the decimation part, requiring 65 multiplications per sample, which is operating at the lowest rate. Both of the CFIR and PFIR are linear-phase construction. A linear phase filter is usually a desirable characteristic in data transmission.

THE OPTIMAL DESIGN OF LINEAR-PHASE FIR DIGITAL FILTERS

According to the theorems that have been discussed in the previous sections, the flow chart in Figure (2) is showing the novel optimum method to minimize the passband error of the linear phase FIR filter and can be applied in multi standards DDC decimation filter with any desirable error in passband ripple in order to reduce the power consumption and simultaneously able to increase the memory size. The PFIR filter is used to optimize the work required to meet the GSM

specifications. The stopband can be set using equations (8,9,10) to allow the deviation (δ_s= 0.01) by assuming a passband ripple Ap ≤ - 0.012 dB , then the passband deviation δP is determined by equation (9) as:

$$\delta_p = \frac{10^{\frac{-0.012}{20}} - 1}{10^{\frac{-0.012}{20}} + 1} \cong 0.0007$$

The filter order is:

$$M = \frac{-20\log(0.01\times 0.0007)^{1/2} - 13}{14.6\,(0.28 - 0.239)} + 1 = 65 \text{ filter length}$$

and

N = M-1 = 65-1 = 64 filter order

Matlab Results

The CIC filter has 5 stages and the decimation factor is 64. The filter exhibits a $|sin(x)/x|^5$ shape. It also has a large DC gain (more than 180 dB), that has to be compensated. The CIC filter was cascaded together with two FIR filters. A 21-tapfilter was used for the polyphase decimator while a 65-taps filter was applied for 65 cycles are required to implement this filter as show in figure3 -4-.

The overall response of the combination from CIC*CFIR*PFIR is shown in Figure(5). The GSM spectral mask requirements are clearly shown in the figure (6). During the filter design, a system-level model of a complete filter chain is automatically generated. This system-level model serves as the golden reference, and allows a direct comparison in simulation results of the HDL code implementation. A direct co-simulation of the system-level golden reference model and the HDL simulator will be useful as a functional mechanism to verify the generated HDL code produces the same results as the original design. In this design, the Simulink in the MathWorks was used as the environment in the model-based design for implementing the test bench. The ModelSim was used to perform the HDL simulations.

In the system-level test bench shows in Fig. 8, there are two signal paths; the first path produces results from the Simulink behavioral model of the three-stage multi-rate

Filter. The second path automatically produces the results VHDL code of the filter chain in ModelSim. During HDL code generation, the hardware and the reset latencies are automatically estimated. These estimations are directly used in the system-level test bench.

The single block ‘filter’ from figure. 8 is actually comprised of three filter stages designed earlier is shown in figure 9.

VERIFICATION RESULTS

In the behavioral model simulation, a block comprises of the three-stage multi-rate filter is designed and placed in the system-level model that can be co-simulated with an HDL simulator. The results were obtained from this co-

simulation from the system-level test bench and the HDL simulator were shown in figure 10.

The trace on the top of figure 10 is the excitation chirp signal. The second trace from the top is an output reference produced by the system-level behavioral model of the three-stage multi-rate filter. The third trace is a result from the co-simulation that generated from VHDL code in the HDL ModelSim simulator.

The last signal shows the per-sample differences between the simulation behavioral model and the synthesizable VHDL code results. As expected, the error is zero for every single sample.

6- Model specifications.

A comparison between the proposed model and other works is show in Table 2. Table shows that most of the parameters were developed and compensated in the new DDC approach to follow the rapid growth in wireless communication system for more effective performance to meet the standard requirements and users demands. The minimum error in passband ripple enable to reduce the power consumption in the filter, and increase the memory size. The clock of the DDC filter can also be improved to allow the filter works with multi-standard and multi-rate such as GSM and WCDMA. This filter also supports all systems that in the frequency band from 50 MHz up to 100 MHZ. The blocker requirement was improved from -105 dB to -117 dB to avoid any interference between GSM signal and other systems. So the DDC filter was developed to accelerate the transition from 3G to 4G.

CONCLUSIONS

In this paper, an emphasize of SDR is a significant technology in 3G and 4G. DDC is a part of SDR, this paper has introduced a novel DDC into the application of GSM base station. A three-stage DDC module for GSM base station is a trade off between the number of stages and complexity. To implement this process, CFIR and PFIR

Filters are applied in the system. The computation and simulation results show that the DDC system is feasible and the filters are effectively more economical in GSM. The methodology to design the Equiripple FIR filter is simple and good approach to obtain the optimal FIR filters with respect to other methods. This technique allows designers to explicit and control the band edge and relative ripple sizes on each band of interest. With this method, the maximum error in passband ripple is about – 0.012 dB and this value is less than the conventional design by -0.018dB. An improvement in the adjacent band rejection and blocker requirements of the filter is present in this paper. A model-based design was used to streamline the process of designing a high-speed digital front-end for an SDR to provide a complete design flow that is possible to be used as a single model for algorithmic exploration. This approach can substantially reduce the cost and simultaneously improve the performance and reliability of RF circuit designs. Therefore the development of the DDC on 3G base station is more economical and effective.

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Symbol	Definition
SDR	**Software defined radio**
GSM	**Global System for Mobile**
WCDMA	**Wideband Code Division Multiple Access**
WiMAX	**Worldwide Interoperability for Microwave Access**
DDC	**Digital Down Converter**
FIR	**Finite impulse response**
FDA	**Filter design and analysis**
HDL	**Hardware description language**
PFIR	**Programmable finite impulse response**
CIC	**Cascaded integrated comb**

Table (1). Parameters of the four type of FIR filters.

Type	I	II	III	IV
Order	Even	odd	Even	odd
F(θ)	1	cos(θ/2)	sin(θ)	sin(θ/2)
M	N/2	(N-1)/2	(N-2)/2	(N-1)/2
θ_0	0	0	π/2	π/2

Table (2): DDC filter specifications comparison.

parameters	GSM mode	WCDMA mode	Researcher [5]	The Proposed DDC
Pass-band ripple	-0.03dB	-0.1dB	- 0.1dB	- 0.012dB
Input format	14 Bit	14 Bit	14bit	16 Bit
Adjacent band rejection.	-30dB	-	-	-35dB
Blocker requirements	-105dB	-	-	-117dB

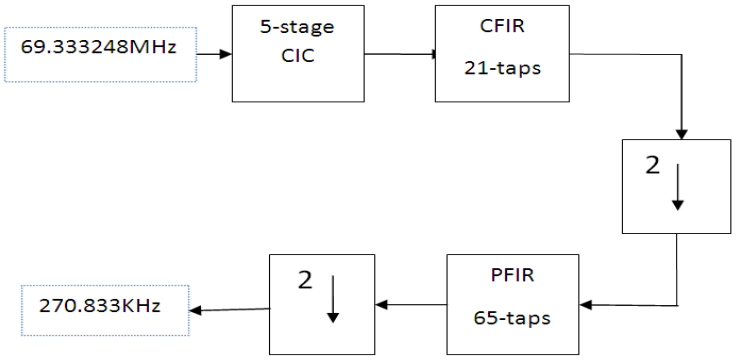

Figure (1): DDC module for GSM based on SDR.

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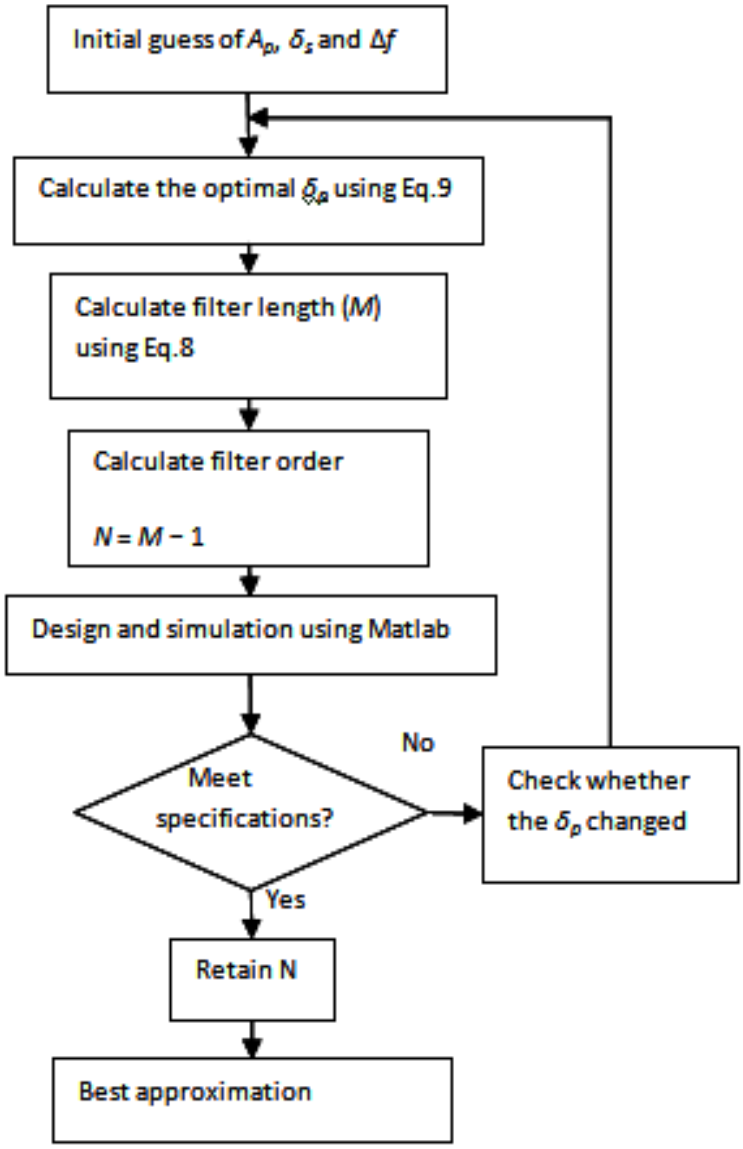


Figure (2): Proposed flow chart of FIR filter design.

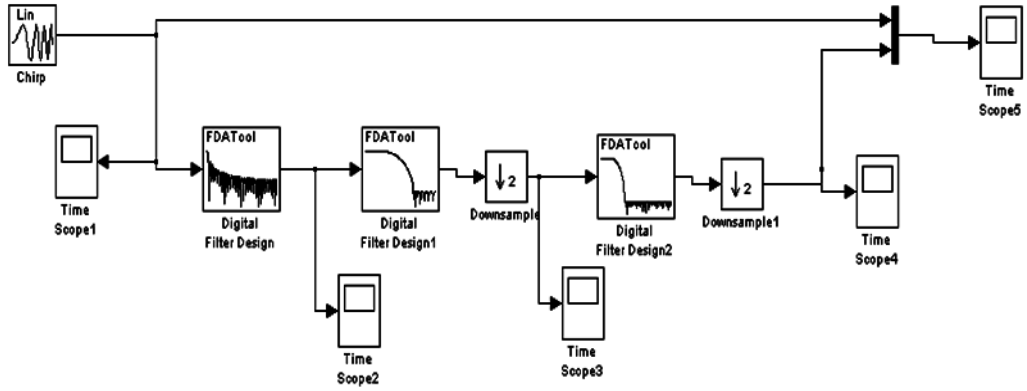


Figure (3): DDC SIMULINK model for GSM mask requirement.

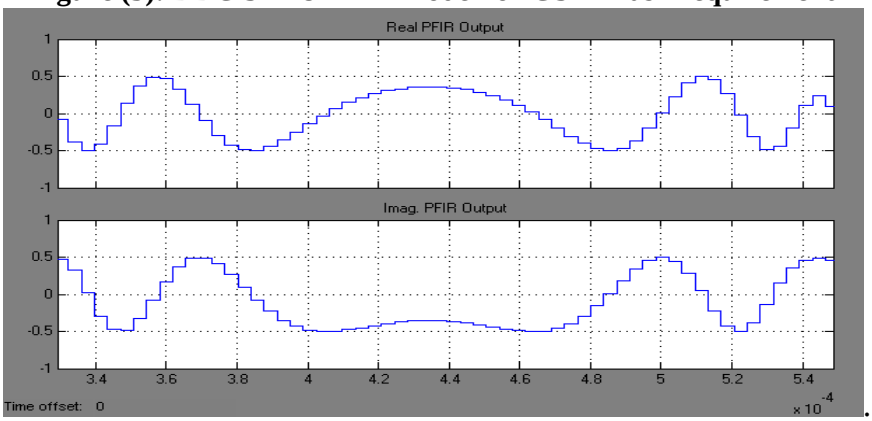


Figure (4): Output GSM signal after PFIR filter.

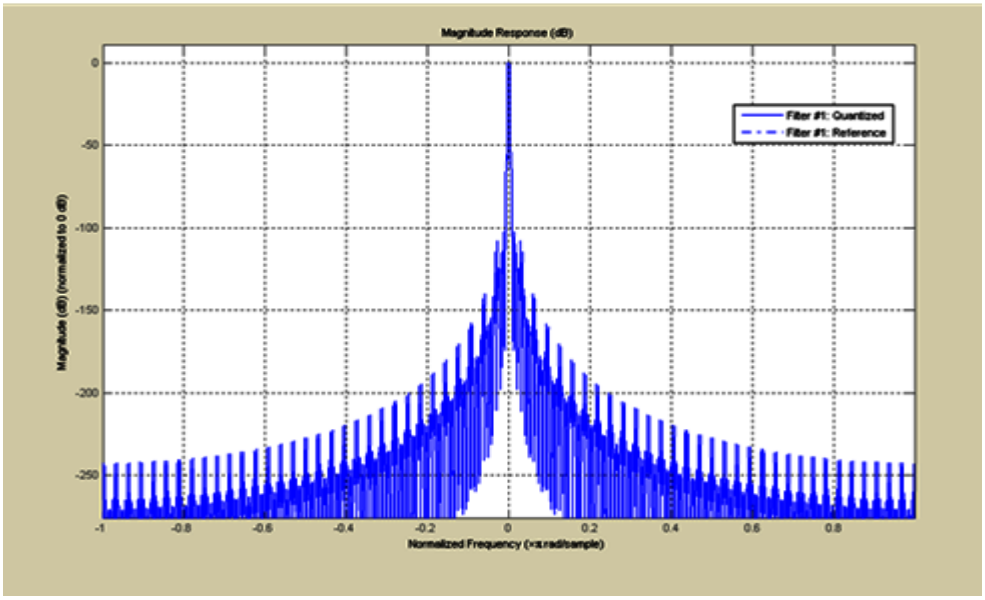
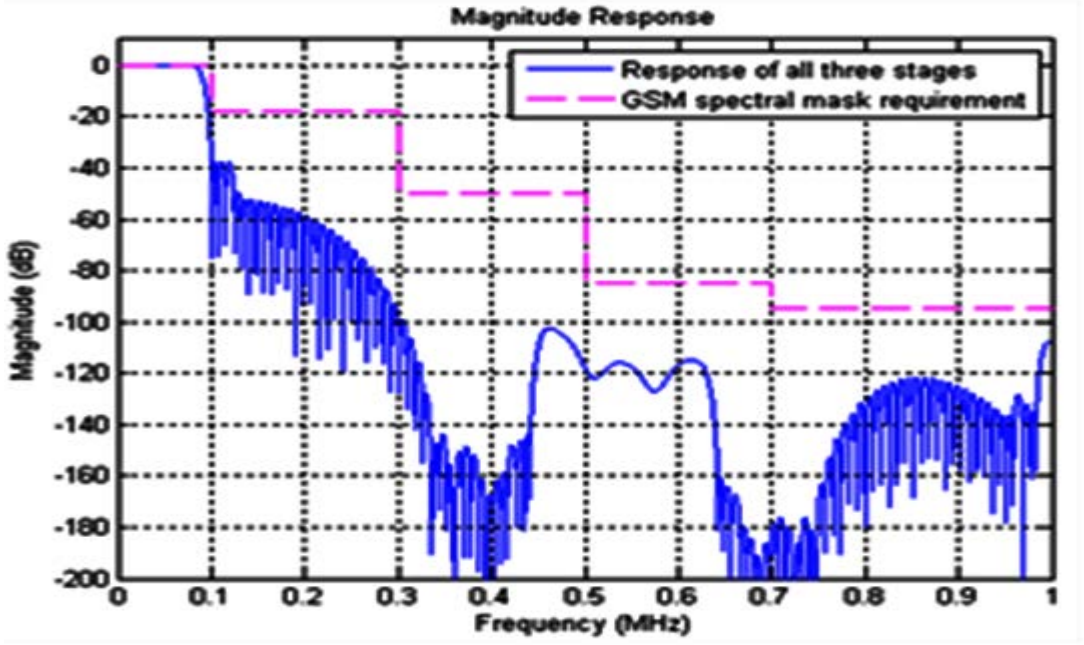


Figure (5): The result from the combination of CIC, CFIR,



Figure(6): The Combination response of CIC, CFIR, and PFIR filters.

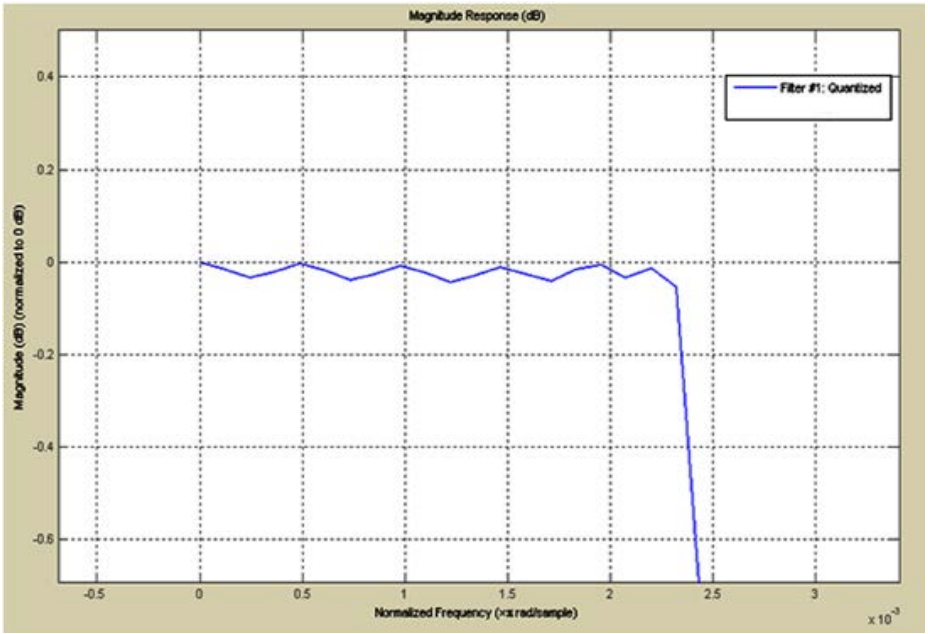


Figure (7): The magnitude response (dB) of the proposal filter after zooming.

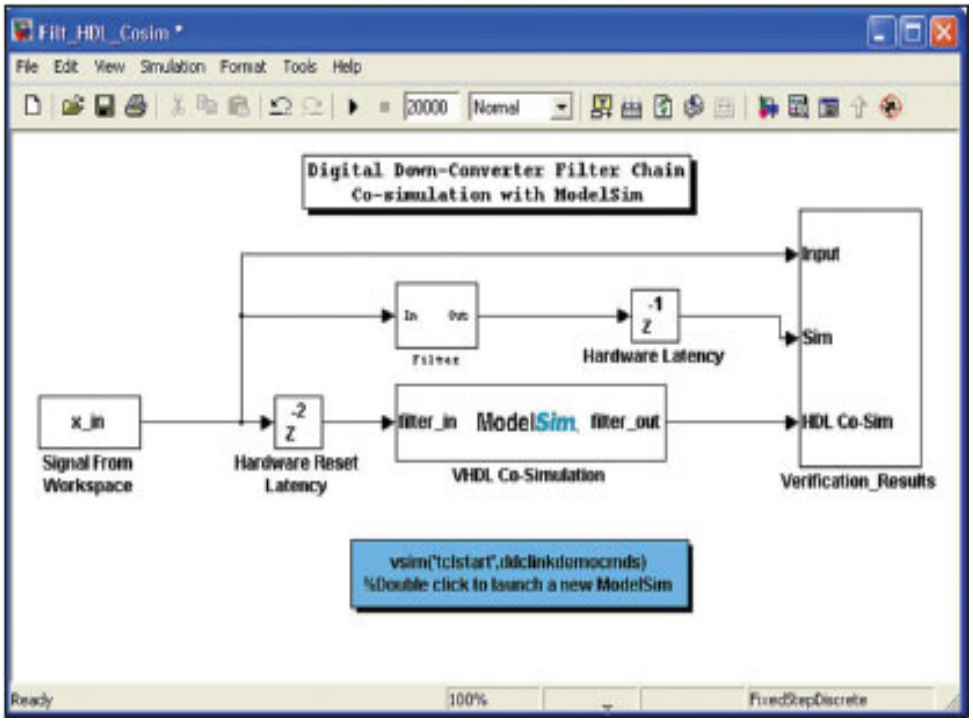


Figure (8): System-level test behch.

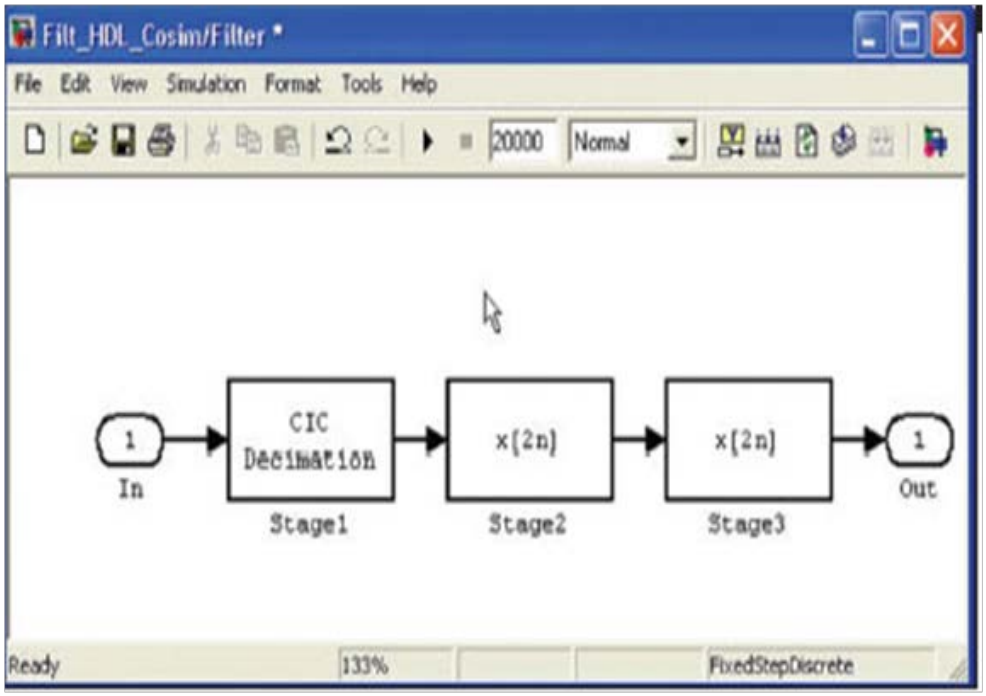


Figure (9): Filter sub-system consisting of the three filter stages.

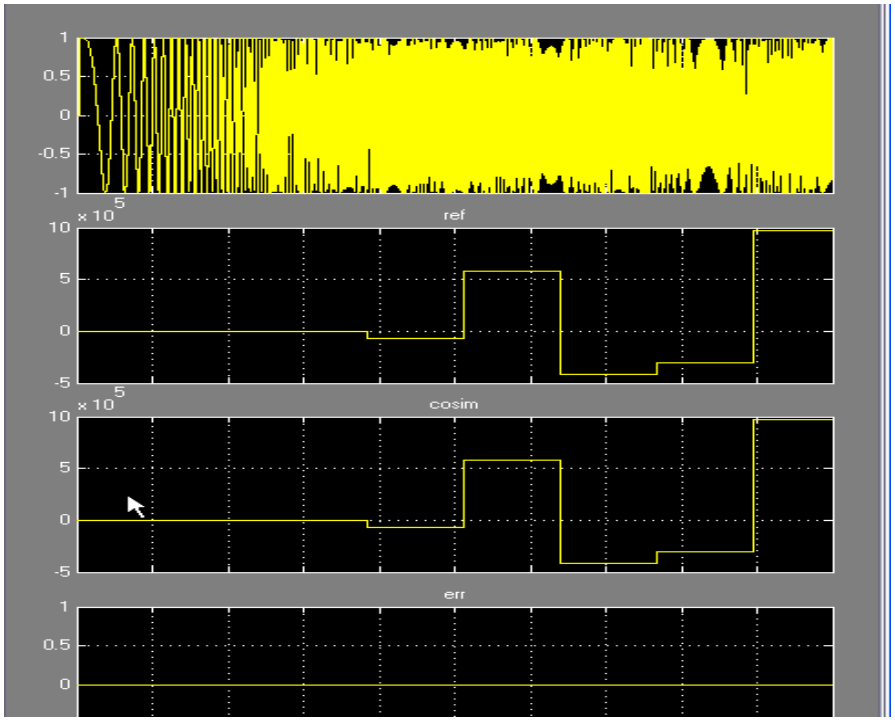


Figure (10). Results from the system-level through co-simulations.